ABSTRACT OF THE DISCLOSURE

A gate driving apparatus for a liquid crystal display includes a shift register which is provided with first and second half-period clock signals having phases inverted with respect to each other and each having a pulse width of a half-period, first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period, a start pulse, a high-level supply voltage and a low-level supply voltage. The shift register generates a half-period output in response to the start pulse and the first and second half-period clock signals. The shift register also generates a one-period output at a half-period delay from an end time of the half-period output in response to any one of the first to fourth one-period clock signals..